

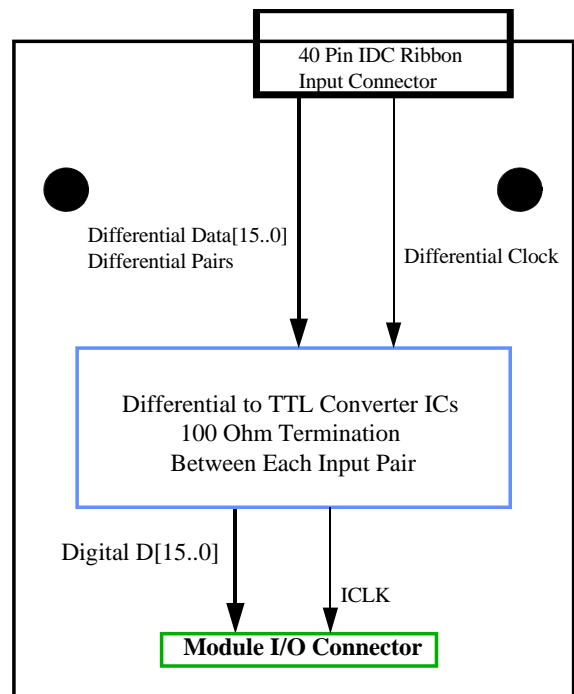
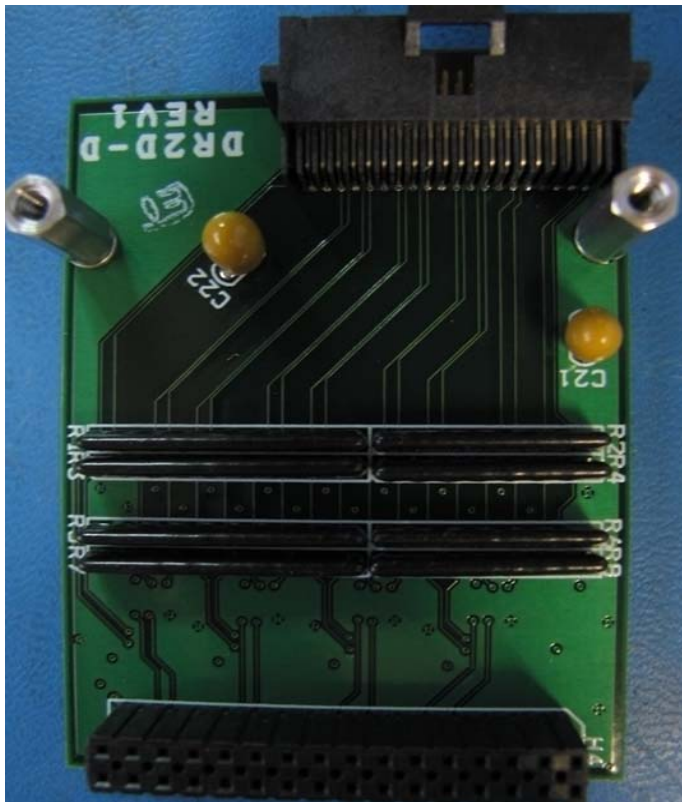
Differential Receiver to Digital rumel, Inc. GIGEXD Input Module

Features

- Uses Differential Data Converters
- 16-bit data plus clock
- -4V to 5V Common Module Input Voltage
- Supports Multiple Differential Logic Inputs
 - 1.LVDS
 - 2.Differential LVECL, ECL
 - 3.Differential LVPECL, PECL
 - 4.Differential LVTTTL, TTL

Applications

- Digital Data To Gigabit Ethernet Transformation
- Digital Data To SDDS Transformation
- Digital Data Time Stamping
- Single channel digital receivers



DR2D-D

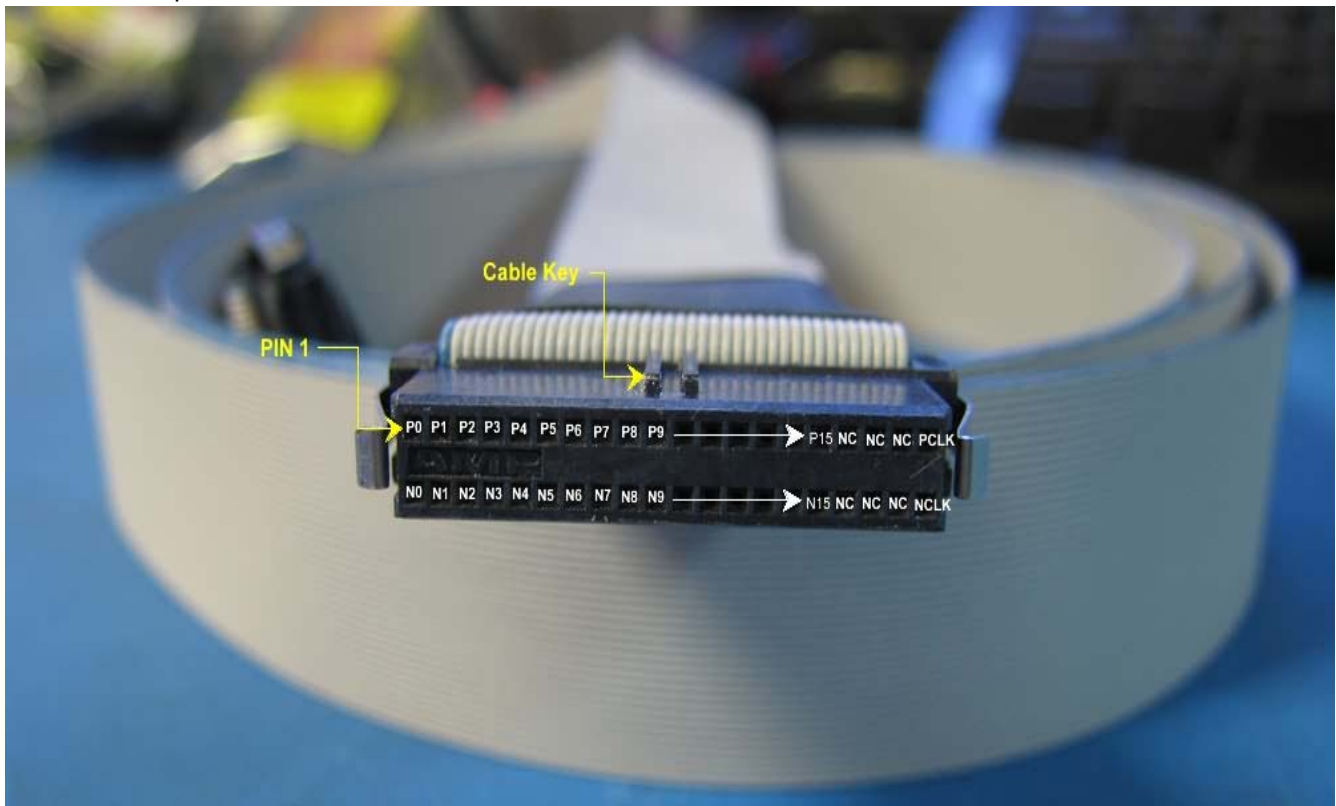
Component Side View

Product Description

The rumel DR2D-D is a 16 bit data plus clock differential receiver module. The DR2D-D module receives differential signals (LVDS, Differential ECL, LVECL, PECL, LVPECL, etc) and converts them to TTL level signals that can be processed by its GIGEXD host. The features for the DR2D-D include the ability to convert any differential signals that have a common mode input voltage in the range of -4V to 5V into standard single ended TTL signals. The DR2D inputs also have +/-50mV of input hysteresis and differential 100 Ohm termination. Input clock rates from 1MHz to 105MHz are supported. Data acquisition on the rising or falling edge of the clock can be configured via the user software interface.

Each unit comes with a 5 ft. cable with a mating IDC connector on each end. There are 3 options for use of this cable.

1. One end interfaces to the DR2D-D module, the other end can optionally be connected to a rumel, Inc. transition panel- that allows for a direct connection to various connector types, SMS/ELCO, SDN/AMP 3x30, etc. Information on various connector transition panels can be found at www.rumel-online.com/products.htm (Note: extension is .htm NOT .html)
2. The user can remove (cut off) the 2nd IDC cable end and then solder on any connector they wish. **NOTE-Data connections should be MSB aligned.** (A wiring diagram is provided near the end of this document.)
3. By contacting rumel, Inc., we can provide cable assemblies to almost any type of connector. Call for an NRE quote/lead time.



NOTE: Differential clock connections PCLK/NCLK must be connected for data acquisition.

DC Electrical Specifications

Parameter	Minimum	Typical	Maximum	Units
Power Supply				
Supply Voltages				
DVcc	3.0	3.3	3.6	V
Supply Current				
I DVcc (DVcc=3.3V)	100	125	150	mA
Differential Inputs				
Va-Voltage at Non-Inverting Input				
Vb-Voltage at Inverting Input				
Vid Absolute Magnitude	0.10		3	V
Vid = Va - Vb				
Vid ≥ -32 mV	2.4		Dvcc	V (Logic Hi)
Vid ≤ -100mV	0		0.8	V (Logic Low)
Open Connections	2.4		Dvcc	Default Hi
Output logic level 0	0		0.8	V
Output logic level 1	DVcc-0.8		DVcc	V

AC Electrical Specifications

			Typical		
Sample clock		1		105	MHz

Notes:

1. Operation below 1 MSPS is possible, with degraded performance

Absolute Maximum Ratings

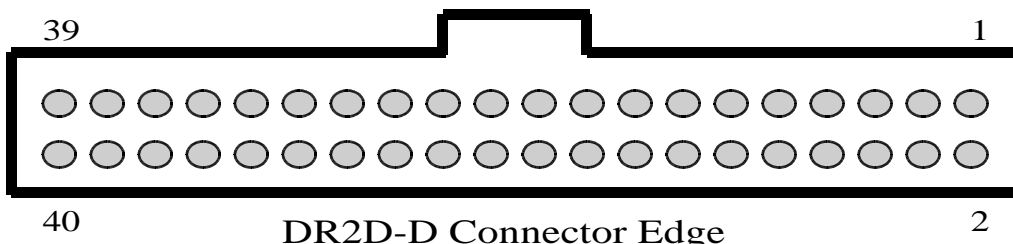
Parameter	Value	Units	Conditions
Electrical			
Dvcc	0 to 4	V	
External Data Input	-4 to 5	V	
Environmental			
Operating Temperature	-10 to +65	Degrees C	
Storage Temperature	-40 to +85	Degrees C	

Note: Operation of this module beyond any of these parameters may cause permanent damage. Exposure to absolute maximum ratings for extended periods may affect module reliability.

Pin Connections

Board header : Type Right Angle IDC, Amp P/N: 104069-6
 Mating Connectors: Type Cable End IDC, Amp P/N: 111196-9
 Mating Cable P/N: ICE-CAB-HD5 (1 provided with GIGEXD/DR2D-D purchase)

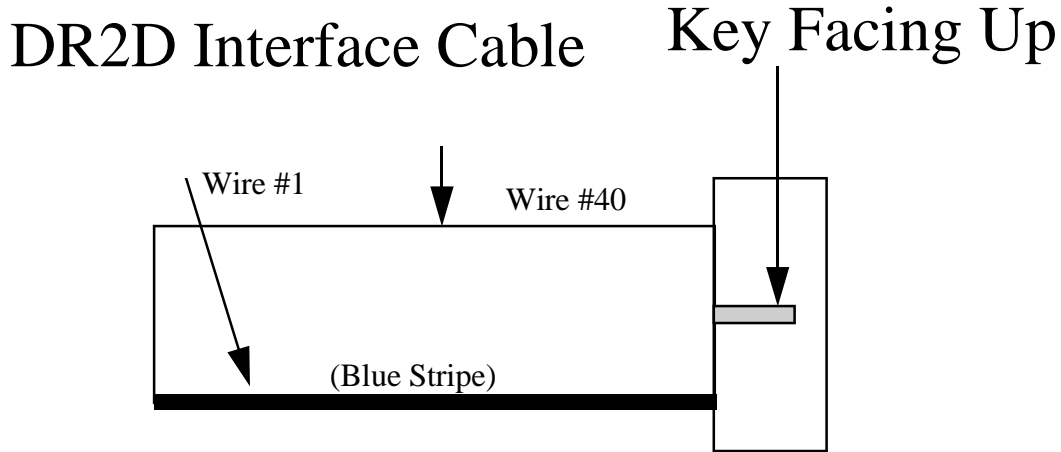
40 Pin IDC Connector Pin Out (DR2D-D)



Note-Data should be MSB Aligned
Signal Definitions On 40 Pin IDC Connector

<u>Pin</u>	<u>Signal</u>	<u>Pin</u>	<u>Signal</u>
1	D0P	21	D10P
2	D0N	22	D10N
3	D1P	23	D11P
4	D1N	24	D11N
5	D2P	25	D12P
6	D2N	26	D12N
7	D3P	27	D13P
8	D3N	28	D13N
9	D4P	29	D14P
10	D4N	30	D14N
11	D5P	31	D15P
12	D5N	32	D15N
13	D6P	33	NC
14	D6N	34	NC
15	D7P	35	NC
16	D7N	36	NC
17	D8P	37	NC
18	D8N	38	NC
19	D9P	39	CLKP
20	D9N	40	CLKN

Cable Connections



Signal Definitions On 40 Pin IDC Connector

Pin	Signal	Pin	Signal
1	D0P	21	D10P
2	D0N	22	D10N
3	D1P	23	D11P
4	D1N	24	D11N
5	D2P	25	D12P
6	D2N	26	D12N
7	D3P	27	D13P
8	D3N	28	D13N
9	D4P	29	D14P
10	D4N	30	D14N
11	D5P	31	D15P
12	D5N	32	D15N
13	D6P	33	NC
14	D6N	34	NC
15	D7P	35	NC
16	D7N	36	NC
17	D8P	37	NC
18	D8N	38	NC
19	D9P	39	CLKP
20	D9N	40	CLKN

IMPORTANT:

1. Data connections should be MSB aligned. For example, if your data source is only 8 bits, then connect to signals D15p/n to D8p/n.
2. CLKp/n MUST ALWAYS be connected to an external clock source.

